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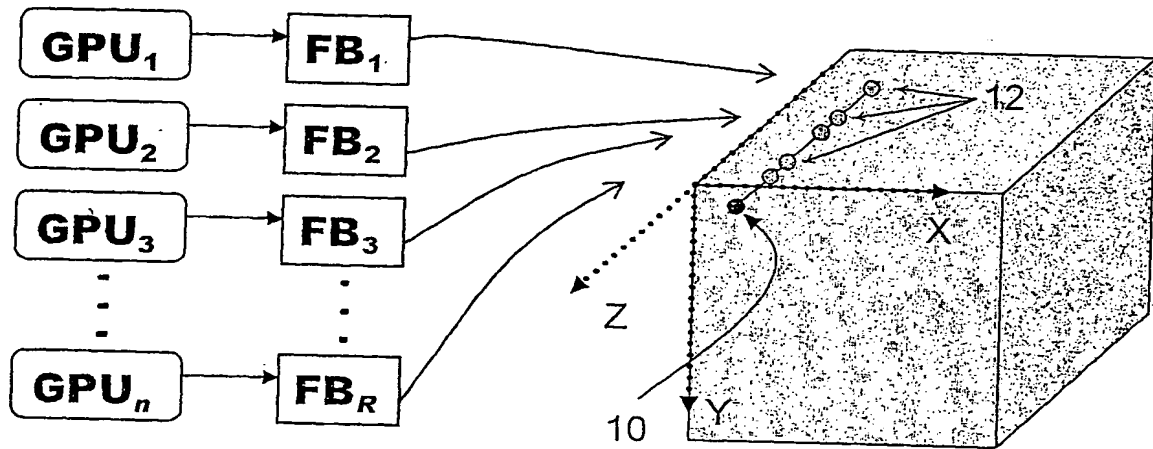


Fig. 1
(Prior Art)

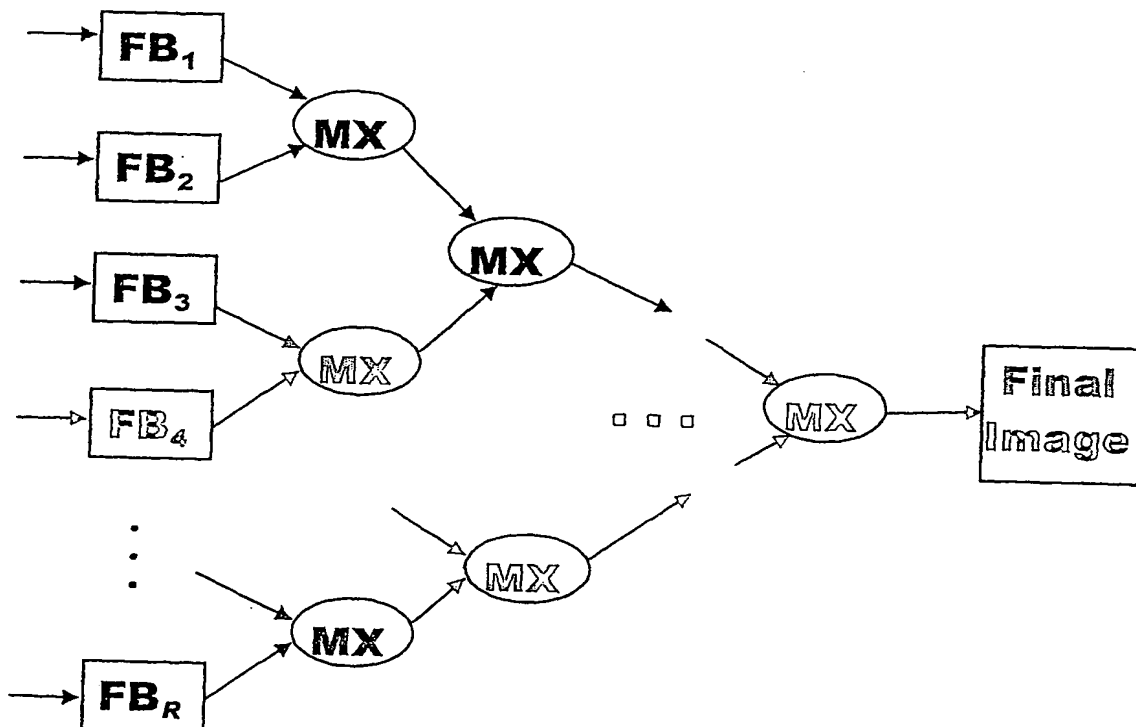


Fig. 2A
(Prior Art)

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Fig. 2B
(Prior Art)

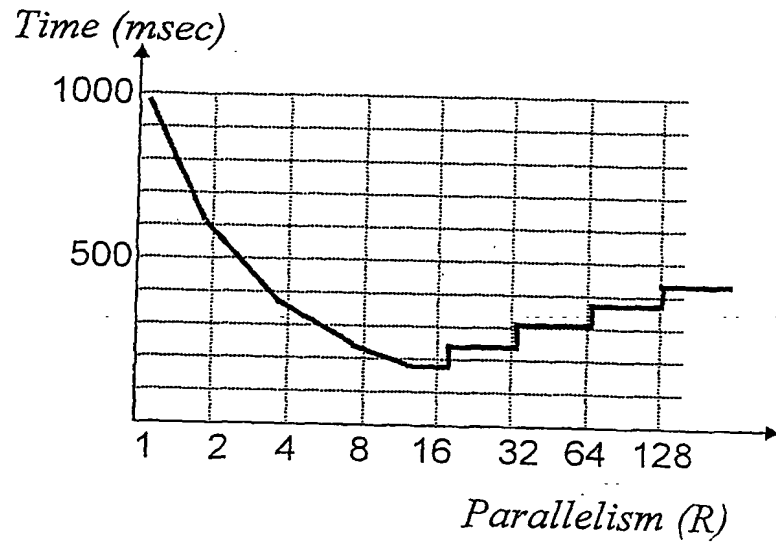
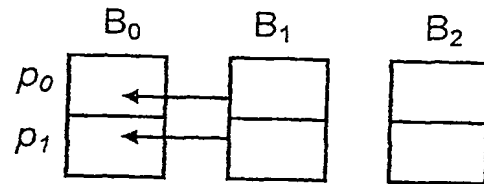


Fig. 3A
(Prior Art)

Stage 1



Stage 2

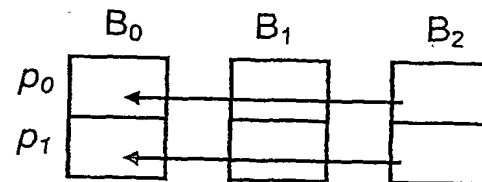


Fig. 3B
(Prior Art)

Do in parallel

let $B = \text{sub-image } i \text{ for processor } p_i$ for $n = 1, 2, 3, \dots, P$ composite sub-images B_0 and B_n

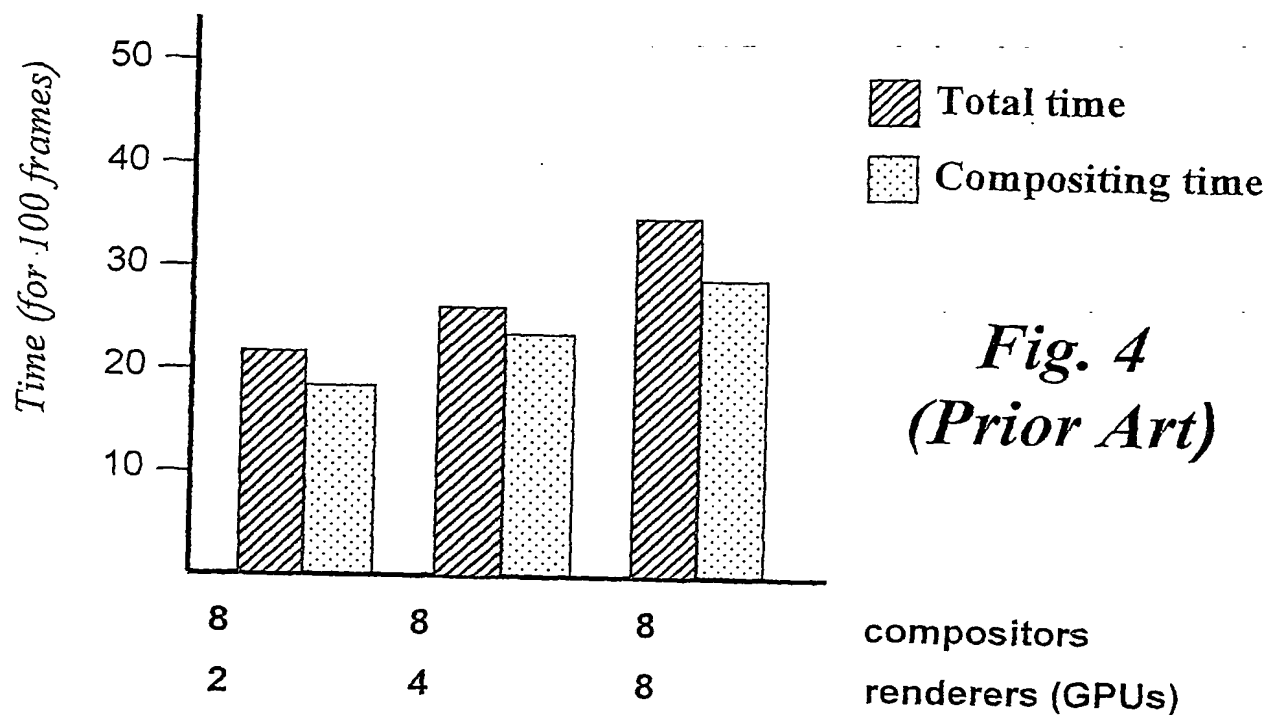


Fig. 4
(Prior Art)

Compositing time for 1024 images.

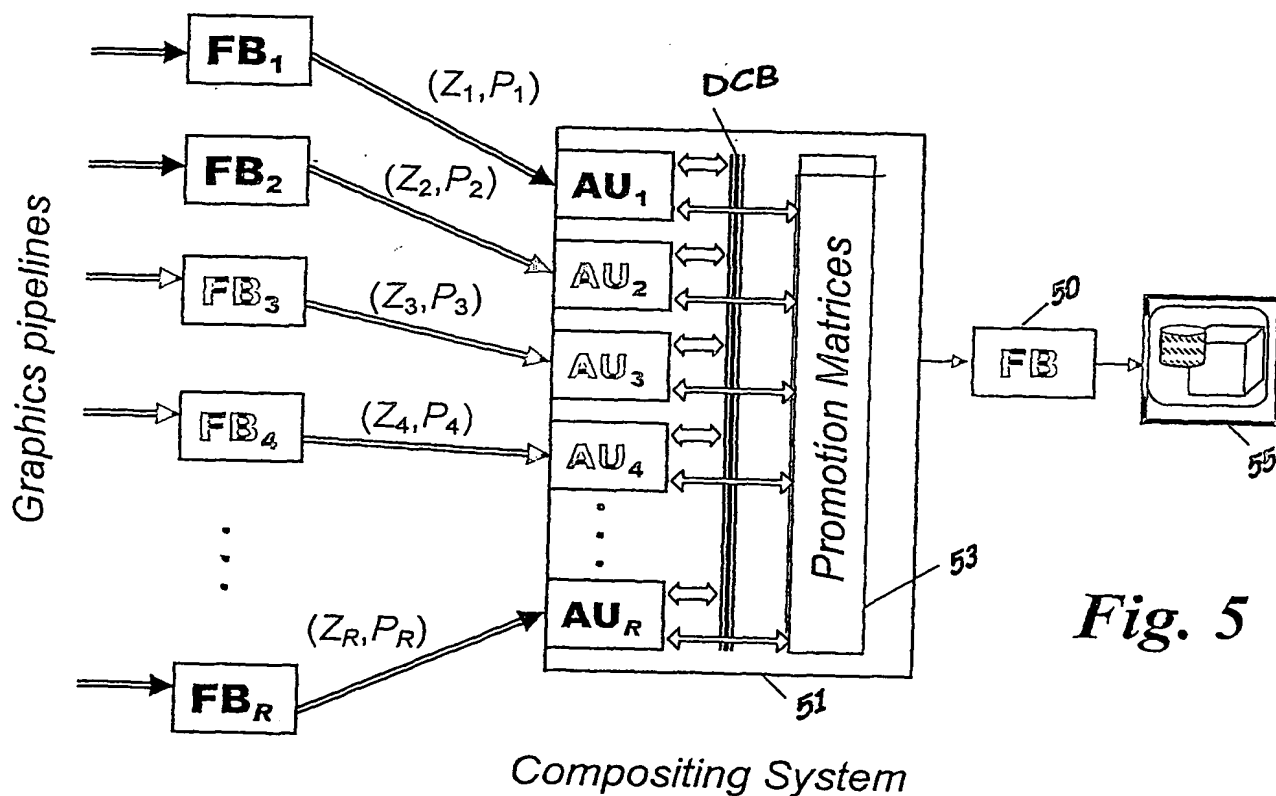


Fig. 5

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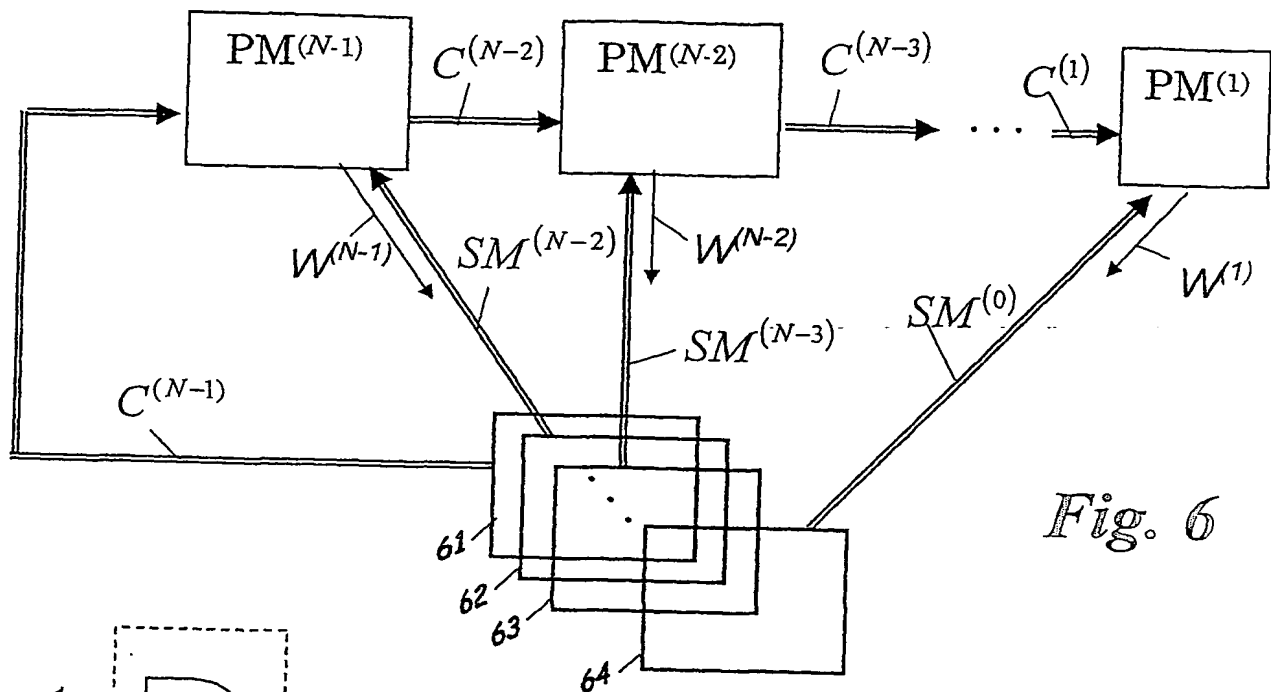


Fig. 6

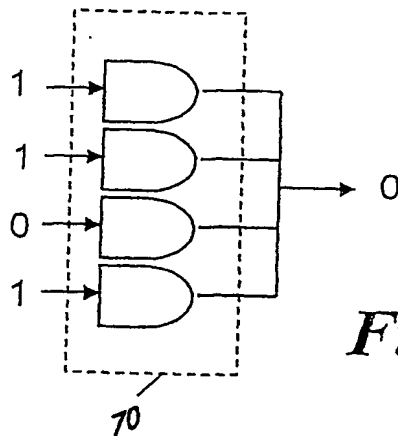


Fig. 7A

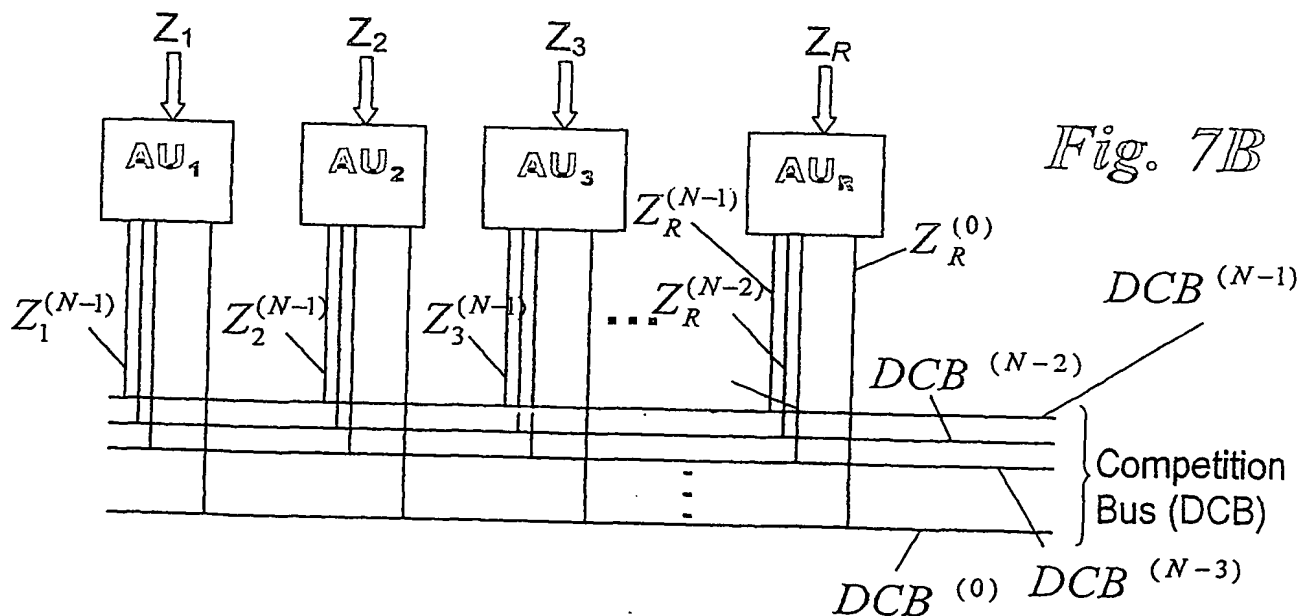


Fig. 7B

From k -th rendering pipeline

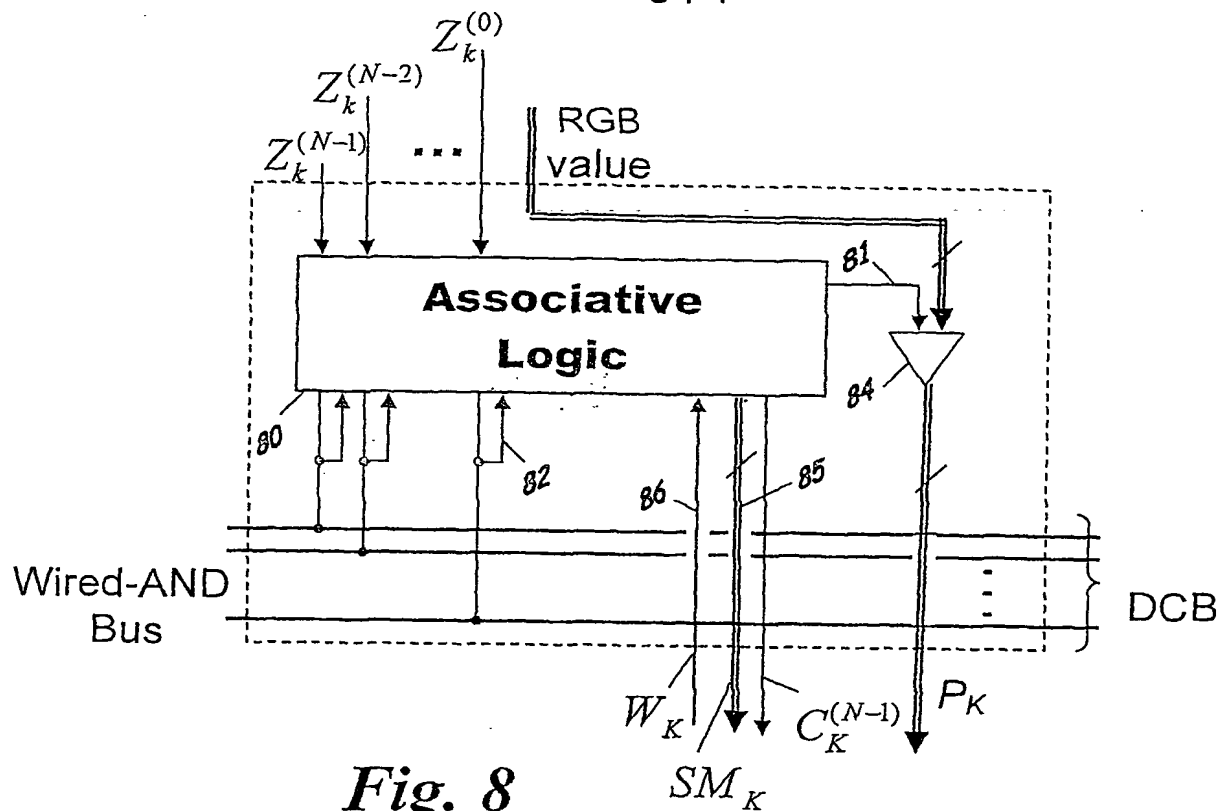


Fig. 8

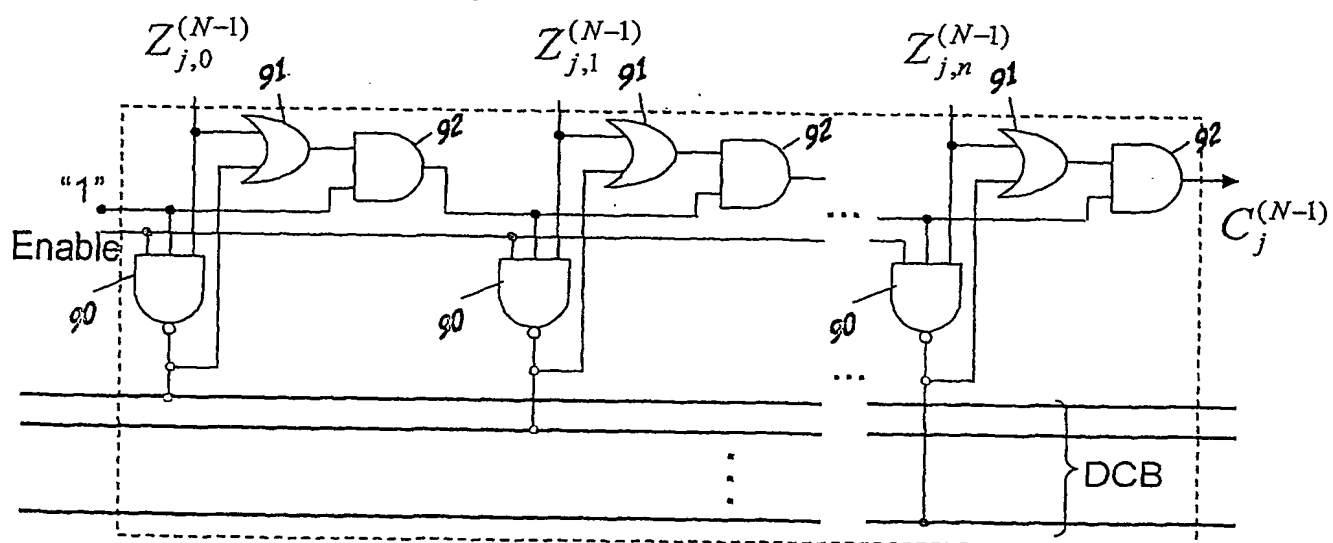
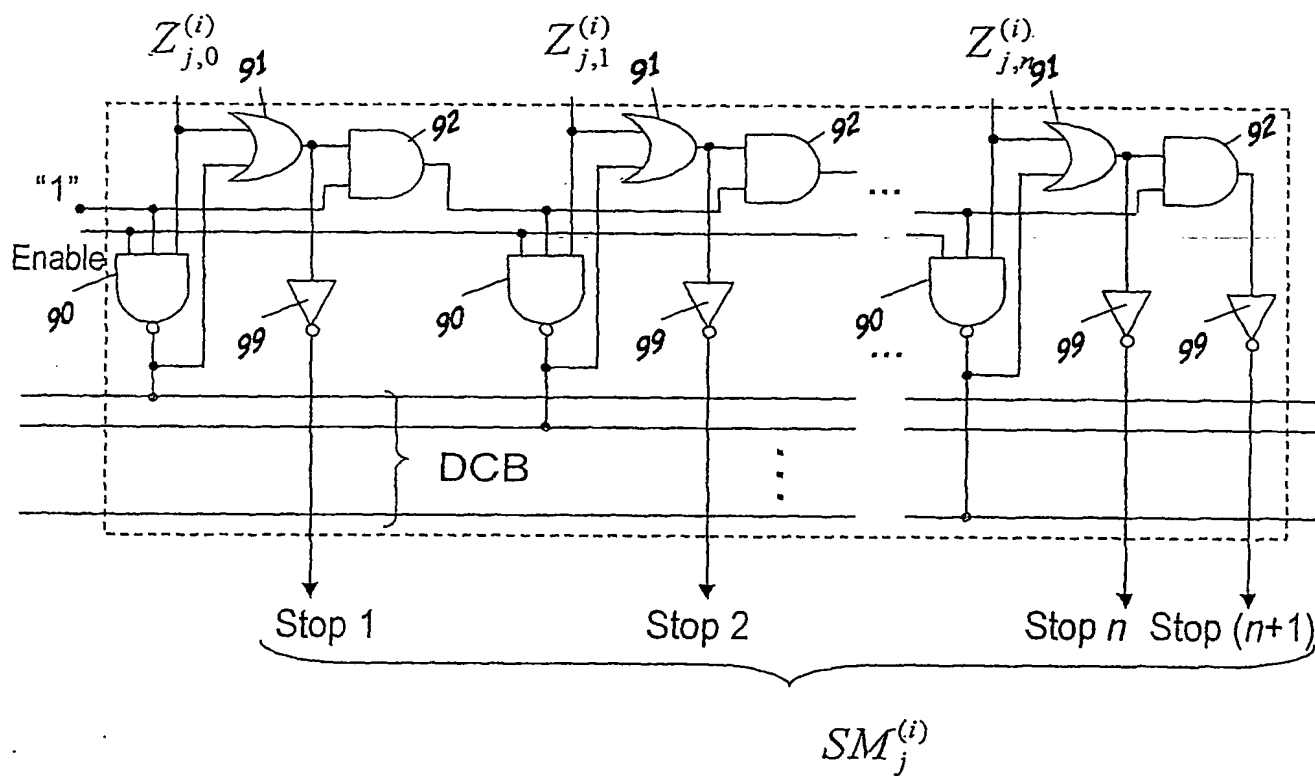


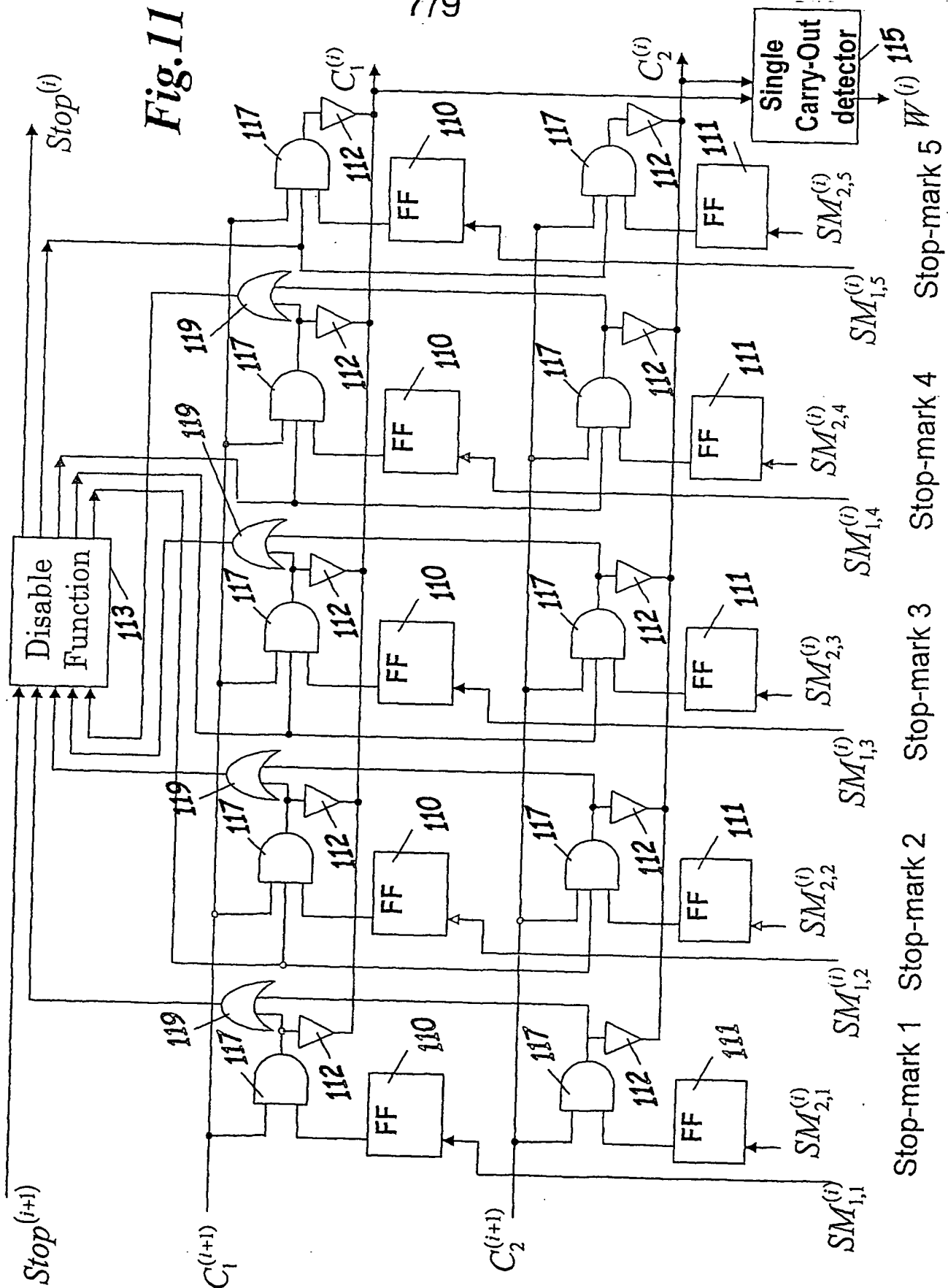
Fig. 9

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**Fig. 10**

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Fig. 11



	Primary segment (8 bits) Carry-out(\rightarrow) or stop	2 nd segment (8 bits) Carry-in, stop- mark, carry-out	3d segment (8 bits) Carry-in, stop- mark, carry-out	4th segment (8 bits) Carry-in, stop- mark, carry-out	Win
a	stop	7	9		
b	\rightarrow	$\rightarrow 9 \rightarrow$	$\rightarrow 9 \rightarrow$	$\rightarrow 8 \rightarrow$	\rightarrow
c	\rightarrow	$\rightarrow 8$	9	7	
d	stop	9	9	7	
e	\rightarrow	$\rightarrow 9 \rightarrow$	$\rightarrow 2$	1	

Z_1 :	10001001	10101000	01000011	11111111	
Z_2 :	10101010	10101011	01000011	11111110	
Z_3 :	10101010	10101010	01000011	11111101	
Z_4 :	10101000	10101011	01000011	11111100	
Z_5 :	10101010	10101011	00111111	00000000	
	$Z_j^{(3)}$	$Z_j^{(2)}$	$Z_j^{(1)}$	$Z_j^{(0)}$	

Fig. 12

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Stack of SIUs

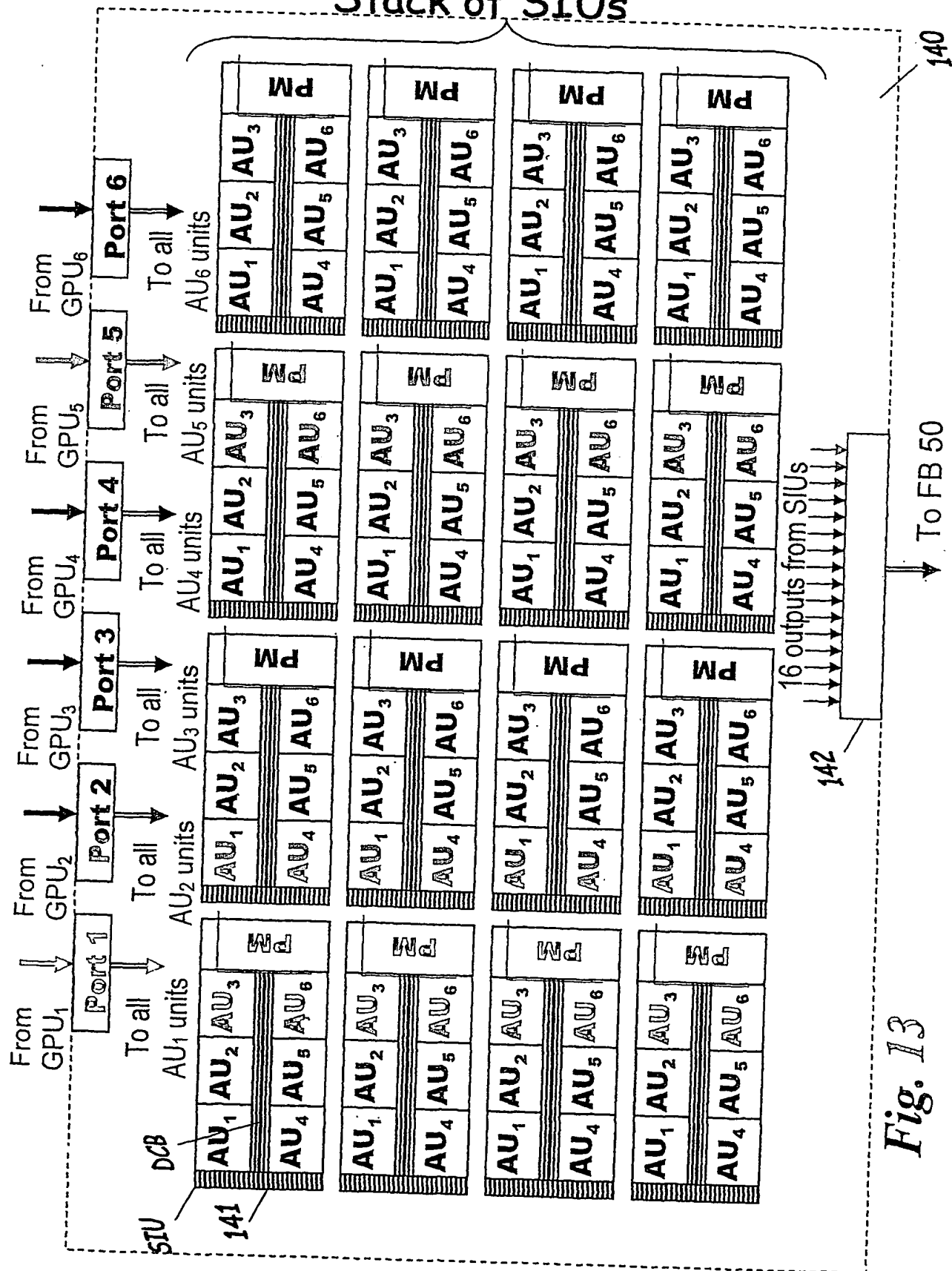


Fig. 13